REMARKS

Summary of Office Action

Claims 1-41 were pending in the above-identified patent application.

The Examiner rejected claims 1-3, 7, 8, 18, 21-23, 27, 28, 30-32, 34, and 37 under 35 U.S.C. § 102(b) as being anticipated by Riley, Jr. U.S. Patent 4,272,729. Claims 19 and 20 were rejected under 35 U.S.C. § 103(a) as being obvious from Riley in view of Berry et al. U.S. patent 6,366,174. Claims 33, 35, 36, and 38-41 were rejected under 35 U.S.C. § 103(a) as being obvious from Jefferson U.S. Patent 5,744,991 in view of Riley. Each of claims 4-6, 9-17, 24-26, and 29 were objected to as depending from a rejected base claim, but allowable subject matter was indicated.

Summary of Applicant's Reply

Applicant notes with appreciation the indication of allowable subject matter in claims 4-6, 9-17, 24-26 and 29, and hereby expressly reserves the right to rewrite any one or more of those claims in independent form should the base claims ultimately not be allowed.

Applicant has canceled claims 1 and 2 without prejudice, rewritten claims 3 and 22 in independent form, amended claims 19-21, 23, 31, 32, and 37 to more particularly define the invention, and added new claims 42 and 43. The claims are fully supported by the specification as filed and no new subject matter has been added.

The Examiner's rejections and objection are respectfully traversed.

Applicant's Reply to the Rejections of Claims 1-3, 7, 8, 18-21, and 31-41

Claims 1-3, 7, 8, 18, 21, 31, 32, 34, and 37 were rejected under 35 U.S.C. § 102(b) as being anticipated by Riley. Claims 19 and 20 were rejected under 35 U.S.C. § 103(a) as being obvious from Riley in view of Berry. Claims 33, 35, 36, and 38-41 were rejected under 35 U.S.C. § 103(a) as being obvious from Jefferson in view of Riley.

Applicant has canceled claims 1 and 2 without prejudice, rewritten claim 3 in independent form, and amended claims 19-21, 31, 32, and 37 to more particularly define the invention. The Examiner's rejections are respectfully traversed.

Independent claim 3 defines a phase-locked loop circuit including, inter alia, a compensation component, a high-gain coarse feedback path for driving the compensation component to within a predetermined variance of a reference signal, and a low-gain fine feedback path for driving the compensation component to lock with the reference signal after the coarse feedback path has driven the compensation component to within the predetermined variance of the reference signal. The coarse feedback path includes a frequency detector and a high-gain signal modifier, while the fine feedback path includes a phase-frequency detector and a low-gain signal modifier.

The phase-frequency detector of the fine feedback path has inputs connected to the reference signal and an output signal, and produces a fine-adjust signal based on a difference between the frequency of the reference signal and the frequency of the output signal. For example, FIG. 1 depicts a phase-locked loop circuit 10, which includes a phase-frequency detector 154 in fine feedback path 151.

In contrast, FIG. 1 of Riley shows a frequency synthesizer 10 and a coarse tuning circuit 24. The Examiner contends that phase detector 18 is a "phase-frequency detector," as defined by applicant's claim 3. Applicant respectfully disagrees. As described in the specification of Riley, "phase detector 18 compares the phase of the divided output signal with that of the reference signal, and produces an analog voltage signal proportional to the phase difference between the two compared signals." Col. 3, lines 63-66. Nowhere does Riley show or suggest a fine feedback path including a phase-frequency detector, where the phase-frequency detector produces a fine-adjust signal based on the difference between an output frequency and a reference frequency, as defined by applicant's amended independent claim 3.

The remaining references do not make up the deficiencies of Riley in failing to show or suggest the claimed phase-frequency detector in a fine feedback path. Berry is cited only for its disclosure of counters in phase-locked loops, while Jefferson is cited only for its disclosure of processing circuitry incorporating a loop circuit. Accordingly, even combining Riley with either or both of Berry and Jefferson would not show the claimed invention.

For at least the reasons set forth above, applicant respectfully submits that amended independent claim 3 is allowable. Accordingly, dependent claims 7, 8, 18-21, and 31-41 are also patentable. Applicant respectfully requests that the rejections to claims 3, 7, 8, 18-21, and 31-41 be withdrawn.

Applicant's Reply to the Rejection of Claims 22, 23, 27, 28, and 30

The Examiner rejected claims 22, 23, 27, 28, and 30 under 35 U.S.C. § 102(b) as being anticipated by Riley. Applicant has rewritten claim 22 in independent form, amended claim 23 to more particularly define the invention, and added new claims 42 and 43. The Examiner's rejection is respectfully traversed.

Independent claim 22 defines a delay-locked loop circuit including, inter alia, a compensation component including a controlled delay line for producing a phase-delayed output signal, a high-gain coarse feedback path for driving the compensation component to within a predetermined variance of a reference signal, and a low-gain fine feedback path for driving the compensation component to lock with the reference signal after the coarse feedback path has driven the compensation component to within the predetermined variance of the reference signal.

The Examiner contends that Riley shows all the elements of applicant's amended independent claim 22. In particular, the Examiner contends that claim 22 has a scope similar to that of claim 2 (now canceled), and phase-locked loop circuits and delay-locked loop circuits are generally interchangeable. Applicant respectfully disagrees. A

phase-locked loop circuit generates an output clock signal whose phase and frequency are both matched to those of a reference clock signal. In contrast, a delay-locked loop circuit accepts as input two existing clock signals whose frequencies are already defined, and aligns only the phase of those two signals. The structure, application, and design of a given loop circuit can vary widely depending on whether it is a phase-locked loop circuit or a delay-locked loop circuit. In addition, applicant's claimed invention, as defined by independent claim 22, includes "a compensation component comprising a controlled delay line for producing [an] output signal, where said output signal is phase-delayed." Nowhere does Riley show or suggest a delay-locked loop including a compensation component with a controlled delay line, a coarse feedback path, and a fine feedback path, as defined in applicant's claim 22.

For at least the reasons set forth above, applicant respectfully submits that independent claim 22 is patentable. Accordingly, dependent claims 23, 27, 28, and 30 and new claims 42 and 43 are also patentable. Applicant respectfully requests that the rejection to claims 22, 23, 27, 28, 30, 42, and 43 be withdrawn and that claims 42 and 43 be allowed.

Applicant's Reply to the Objection of
Claims 4-6, 9-17, 19, 20, 24-26 and 29

For at least the reasons set forth above, applicant respectfully submits that independent claims 3 and 22 are patentable. Accordingly, each of dependent claims 4-6, 9-17, 19, 20, 24-26 and 29 should also be patentable.

Conclusion

For the reasons set forth above, applicant respectfully submits that this application is in condition

for allowance. Reconsideration and prompt allowance of this application are respectfully requested.

Respectfully submitted,

Jeffrey H. Ingerman
Reg. No. 31,069
Attorney for Applicant
FISH & NEAVE IP GROUP
ROPES & GRAY LLP
Customer No. 36981
1251 Avenue of the Americas
New York, New York 10020-1105
Tel.: (212) 596-9000